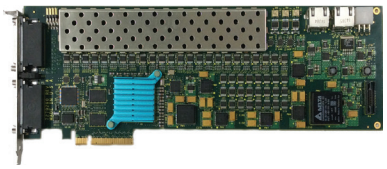
Engine Sensor Simulation PCIe Card

The Engine Sensor Simulation Card is a customized version of Concurrent's programmable FPGA card especially designed for hardware-in-the-loop engine control unit (ECU) testing. The card and its associated firmware can support two- and four-cycle engines with up to sixteen cylinders and four independent, variable-phase camshafts. Engine speeds up to 30,000 rpm with .001 rpm resolution can be simulated along with crank reverse rotation (idling stop).

In HIL engine testing, an ECU is connected to a real-time simulation computer that executes the engine model and evaluates the ECU's operation. An engine ECU handles a wide variety of input and output control signals that perform on the microsecond level. A single high-performance FPGA card, with its customizable firmware, can often provide an interface to the ECU that would otherwise require multiple standard data acquisition cards. An FPGA I/O card can also buffer ECU events to provide improved performance communication to and from the simulation model.



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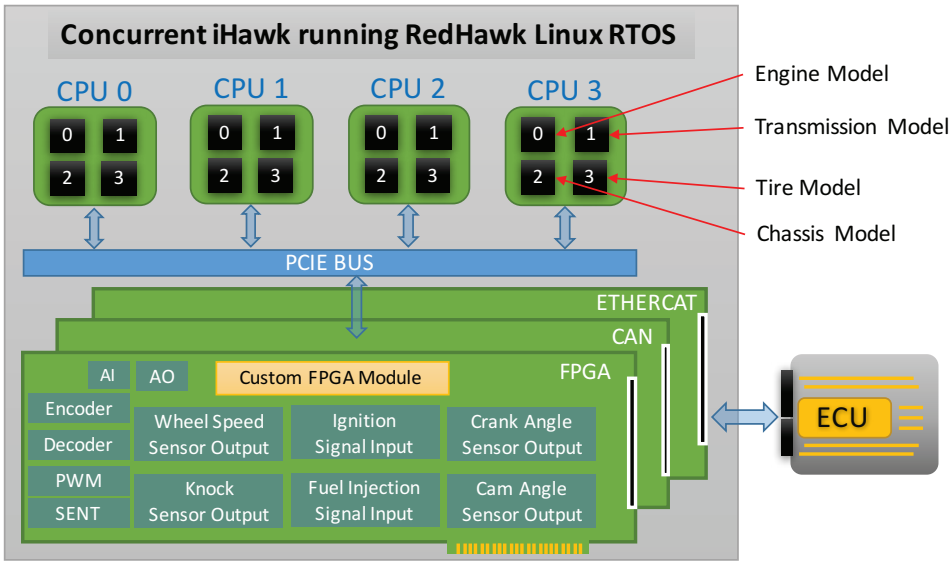
Current FPGA Technology

Concurrent's family of programmable FPGA PCIe cards feature a powerful field programmable gate array that supports both digital and analog I/O. The card can control up to 96 digital I/O signals along with sixteen 16-bit analog inputs and sixteen 16-bit analog outputs. The FPGA card features isolated I/O power, high-speed digital isolators and multi-board synchronization. Optional NIST traceable calibration is available for the analog section. The card's I/O functionality can be customized by the user by means of an FPGA development tool kit. For advanced requirements, Concurrent's family of cards includes a range of powerful FPGAs containing up to 504,000 logic elements.

SIMulation Workbench Modeling Environment

The Engine Sensor Simulation FPGA card is fully supported by Concurrent's SIMulation Workbench™ (SimWB), a comprehensive framework for developing and executing real-time HIL simulations. The SimWB real-time core is organized around a very fast memory resident database (RTDB). Simulation models and I/O processes have direct access to the RTDB with very low latency. Models and I/O processes run sequentially during a real-time loop with their execution dispatched by the SimWB scheduler. This modular design allows for complete I/O independence for the various models using a point-and-click GUI. SimWB provides scalability across multiple cores as the number of simulation models and hardware I/O devices increase. SimWB fully leverages the powerful features of Concurrent's RedHawk™ Linux® real-time operating system.



Firmware Specifications

- Generation of Crank-Angle Sensor Signals
  - Arbitrary Pulse Pattern Configuration with less than 0.006° CA Resolution at + 30,000 RPM
  - Waveform generation identifiable by crank reverse rotation
    - Phase Shifting Output (A/B-Phase)
    - Multi-level Voltage Output
    - Pulse Frequency Modulation Output
- Generation of Cam-Angle Sensor Signals
  - Waveforms up to 4 Shafts
  - Arbitrary Pulse Pattern Configuration with less than 0.006° CA Resolution for each shaft
  - Synchronization with Crank-Angle
  - Individual Phase Variable Command for all shafts (resolution 0.01°CA)
- Acquisition of Ignition Signals
  - Up to 16 channel inputs
  - Acquire the leading/trailing-edge timing of Crank-Angle sensor base
  - Minimum pulse width 50 nanosecs
  - Multiple pulses can be buffered
- Acquisition of Fuel Injection Signals
  - Up to 16 channel inputs
  - Acquire the leading/trailing-edge timing of Crank-Angle sensor base
  - Minimum pulse width 50 nanosecs
  - Multiple pulses can be buffered
- Operation from SIMulation Workbench configuration
  - I/O configuration independent of modeling tools

Hardware Specifications

- 96-channel Digital I/O
  - 5V 4mA TTL (3.3V Available)
  - Digital I/O Direction per Nibble
  - High Speed Digital Isolators
- 16-channel 16-bit D-to-A Conversion
  - Single-ended Output
  - 0 to +10V, +/-5V or +/-10V Output
  - Range Selection
  - 10 Milliamp Output Drive
  - 100K Updates/sec per channel
- 16-channel 16-bit A-to-D Conversion
  - Differential or Single-ended Input
  - +/-5V or +/-10V Input Range
  - 300K Updates/sec per channel
- Altera Arria V Family FPGA
  - 362K Logic Elements
- 1GB DRAM
- TCXO Clock Source
- 8-output Programmable Clock Generator
- Industry Standard SCSI 68-pin VHD Connectors for I/O
- RJ-45 Connectors for Multi-board Synchronization
- PCI Express x4 Revision 1.0a
- Isolated Power on all I/O
- Optional NIST Traceable Calibration
- Packaging
  - Full Height Full Length PCI Express (12.3" long x 3.8" high)
- Power Requirements
  - Up to 25 watts (12VDC @ 2 Amp) without external power connector
  - Up to 60 watts with external power connector
- Environmental
  - Operating: 10° to 40° C
  - Storage: -40° to 65° C
  - Relative Humidity: 10 to 80% noncondensing
  - Cooling: Forced Air Required
  - ROHS Compliant

Ordering Information

- CP-ENG-SIM
  PCIe x4 card with 96-channel 5V Digital I/O, 16-channel Analog Out, 16-channel Analog In
- WC-CP-FIO
  Driver for RedHawk Linux
- ICS-SWB-1277
  SIMulation Workbench I/O License